On the usage of Actel IGLOO FPGAs for CubeSat applications

Introduction

CubeSat

A CubeSat is a type of miniaturized satellite for space research that usually has a volume of exactly one liter (10 cm^3), has a mass of no more than 1.33 kg. CubeSats can be launched from standard containers on the side of larger satellite launch flights.

One of the advantages of CubeSat is the low price. So it is important to reach the mission objectives while keeping the budget low. The CubeSat will work in the space, but the reliability requirements are leveraged and the choice of electronic components is not limited to the radiation hardened parts usually found in satellite design.

Nevertheless, new CubeSat designs tend to choose electronic components already used in previous pico- and nanosatellites designs. A few missions incorporate totally new devices, in particular for low priority functions. If the component proves to function successfully, it will be re-used in further CubeSat designs.

Radiation effects for space electronics

The followings are some aspects about problems caused by radiation in electronic circuits [nasW]:

- total ionizing dose (TID)
- single event transients (SET)
- single-event upsets (SEU)
- single-event latchup (SEL)

SET and SEU are also refferred as Single Event Effects (SEE).

Total ionizing dose affect the functionality of an semiconductor circuit. High enery particles change the arrangement of the atoms in the crystal lattice. This increases the number of recombination centers, depletes the minority carriers and worsenes the properties of the affected semiconductor junctions. In CMOS devices, the radiation also creates electron–hole pairs in the gate insulation layers, which biases the threshold voltages of the transistors.

Single event tansients occur when high-energy ionizing particles, such as heavy ions, alpha particles or protons, irradiate a circuit or pass through an integrated circuit causing a disruption in the system logic.

Single event upsets occur upon SET events and are seen as the change of the logic value stored in a memory element such as a fliflop (FF) or a Random Access memory (RAM). In sysnchronous designs, SET either happen between two rising clock edges and do not interfere with the normal functioning of the device, or they happen at the clock time or inside the memory element and are treated as SEUs.

Single event latchup is a condition that causes loss of device functionality due to a high current induced in a parasitic PMOS and NMOS transistor pair. Once this current is started, the transistor pair permanently amplifies it, and the only way to resume to a normal operation is to power-off the circuit. A SEL may or may not cause permanent damage.

Actel IGLOO FPGA circuits

Contrarily to microprocessors, Field-Programmable Gate Arrays (FPGAs) can be configured to incorporate logic for the mitigation of SEU effects. Mitigating the effect of a bit flip in a microprocessor running an Operating System (OS) is a much more difficult task.

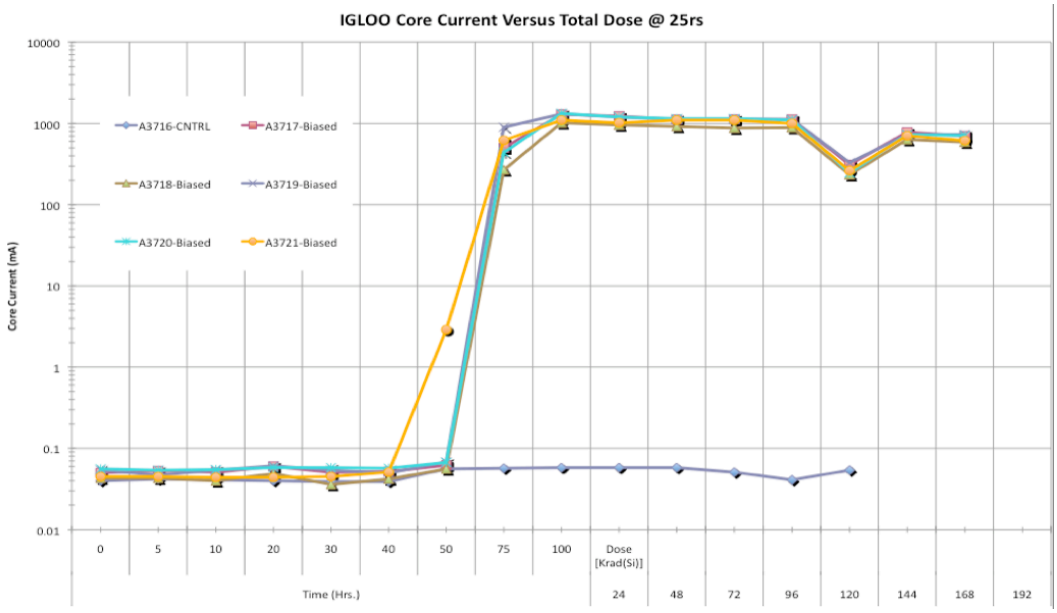
Additionally, the FPGA power consumption can be monitored to promptly react to SEL occurrences which could affect these devices.

Actel FPGAs, part of Microsemi SoC Product Group's portfolio, include the RT family of radiation tolerant devices. These circuits are very expensive, and effort has been made to study the immunity of the Custom Off-The-Shelf (COTS) Actel IGLOO family [rez07], [jpl08]. Additionally, Aeroflex Gaisler AB have a telemetry encoder and telecommand decoder implemented in an IGLOO FPGA in their product portfolio [Gai09].

Ionizing dose

The Jet Propulsion Lab has made a measurement campain to characterize the TID resilience of COTS Actel FPGA circuits [jpl08]. All devices were irradiated at a dose rate of 25 rad(Si)/sec at room temperature.

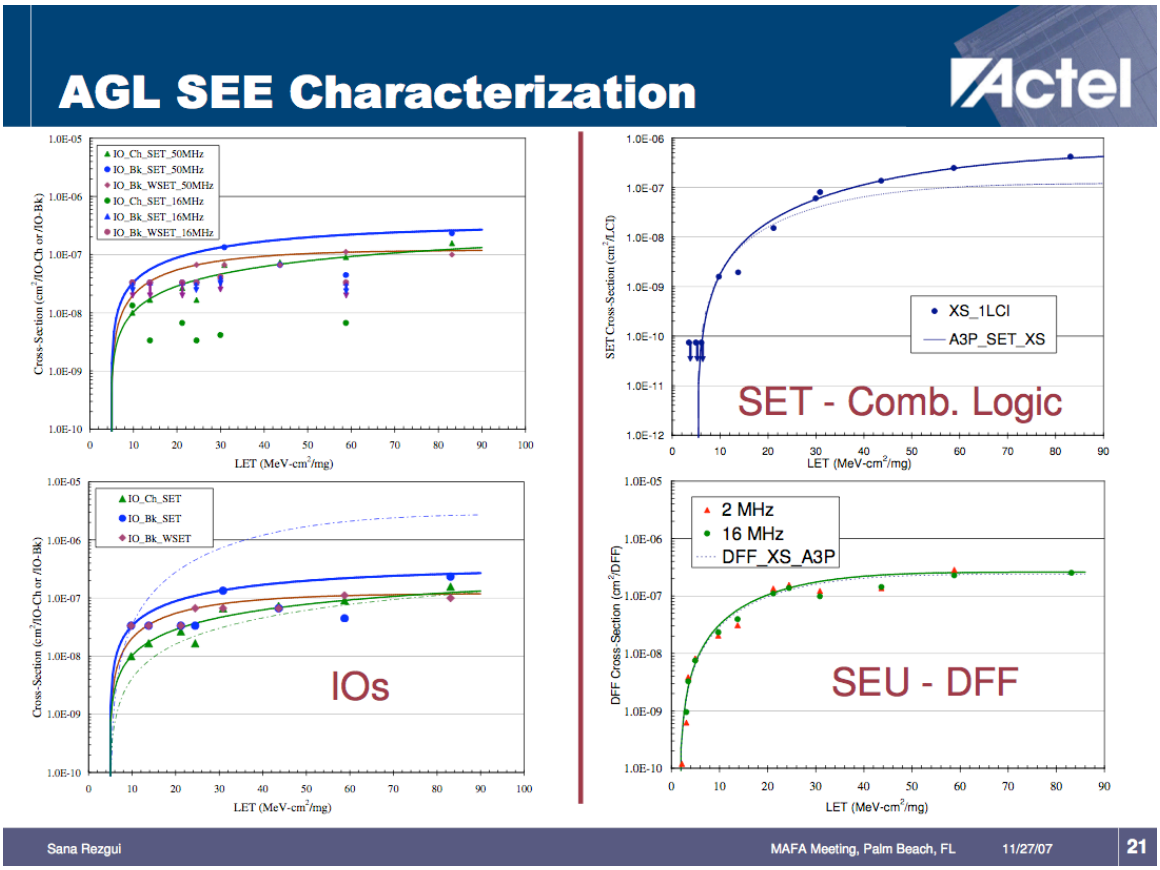
The following picture from [jpl08] shows that the IGLOO devices all withstood a dose of 40 krad(Si).



For their telemetry and telecommand circuit [Gai09], Aeroflex Gaisler specify a total ionizing dose up to 10 krad(Si).

SEE mitigation

Actel have characterized both their ProASIC3 and IGLOO FPGA technologies. Results from [rez07] for IGLOO devices are shown in the following figure:



In these figures, the cross-sections provide an information about the SEE probability: multiplying this surface, in [m^2 / bit], by the energy flux density, in [1 / (m^2·sr·s)], and the exposed solid angle , in [sr], gives the SEE rate, in [1 / (s·bit)].

Actel have identified the following radiation issues for the ProASIC3 and IGLOO technologies:

- PLLs have a programmable frequency ratio and can be upset by SEU
- on-chip RAM is very sensitive to SEU
- flip-flops are sensitive to SEU
- I/O bank configuration is sensitive to SEU
- combinatorial logic is sensitive to SET, leading to SEU in flip-flops

SEU mitigation can be used as in the Aeroflex Gaisler telemetry and telecommand circuit [Gai09]. This bases on the following ideas:

- not using the PLL
- using EDAC to correct errors in the on-chip RAMs
- using TMR or similar on flip-flops (some synthesis tools provide this as an option)
- triplicating all inputs and using majority voting, triplicating all outputs and let the next circuit handle the majority voting
- using a clock frequency as low as possible to avoid SET effects as much as possible
- providing in-orbit reprogramming capabilities, in order to cope for configuration changes due to SEU

For the last point, let us note that bit changes in the FPGA configuration EEPROM are as likely as bit changes in a microprocessor program EEPROM.

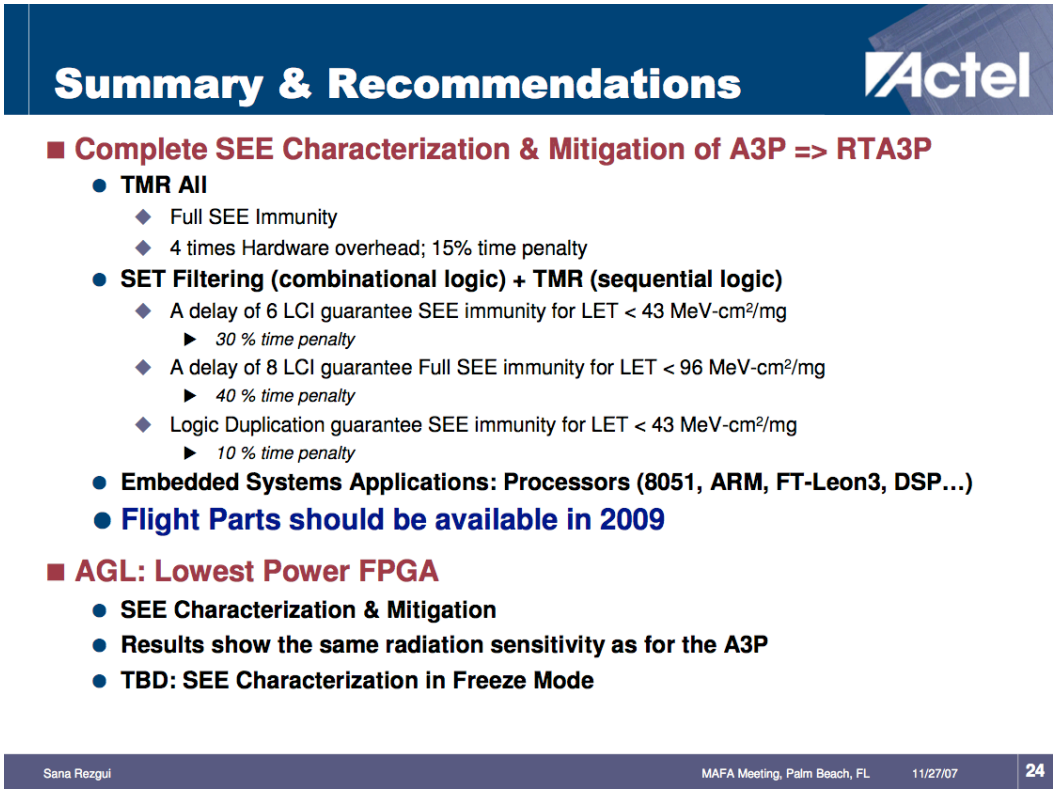
With these mitigation techniques, Aeroflex Gaisler state that their telemetry and telecommand circuit [Gai09] is immune to SEU for LETth > 0 MeV-cm2/mg (i.e. any LET).

Latchup

In the specifications of their telemetry and telecommand circuit [Gai09], Aeroflex Gaisler state that the device is immune to SEL for LETth > 0 MeV-cm2/mg (i.e. any LET).

Conclusions

A summary from [rez07] for ProASIC3 and IGLOO devices is shown in the following figure:



With this, one can consider that :

- IGLOO devices support TID of 10 to 40 krad(Si)
- with proper mitigation techniques, one can achieve full SEE immunity
- the IGLOO technology is immune ti SEL
- SEU might happen in the FPGA configuration EEPROM but in a similar way as it would happen in microprocessor program EEPROM.

It is to be noted that the SEE characterization has not been done for IGLOO devices put in freeze mode. As the energy consumption is dramatically reduced in this mode, one can also expect that the energy required to produce an SEU would be reduced as well.

References

[nasW] "Single Event Effects Specification", NASA/GSFC Radiation Effects & Analysis Home Page, <http://radhome.gsfc.nasa.gov/radhome/papers/seespec.htm>

[rez07] S. Rezgui, J.J. Wang, Y. Sun, B. Cronquist and J. McCollum, "New Reprogrammable & Non-Volatile Radiation Tolerant FPGA RTA3P - Low Power", Military and Aerospace FPGA and Applications (MAFA) Meeting, November 2007, <https://nepp.nasa.gov/mapld_2008/presentations/ w/10%20-%20Allen_Gregory_mapld08_pres_1.pdf>

[jpl08] G. Allen, S. McClure, S. Rezgui, and J.J. Wang, "Total ionizing dose characterization results of Actel ProAsic3, ProAsic3L, and IGLOO Flash-based FPGA", The Jet Propulsion Laboratory, California Institute of Technology and Actel Corporation, September 2008, <https://nepp.nasa.gov/mapld_2008/presentations/ w/10%20-%20Allen_Gregory_mapld08_pres_1.pdf>

[Gai09] Aeroflex Gaisler AB, "GR-TMTC-0001 Telemetry & Telecommand", December 2009, <http://www.gaisler.com/index.php/products/components/gr-tmtc-0001>